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EXAMINER	
BAHTA, KIDEST	

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,440	MAHER ET AL.	
	Examiner	Art Unit	
	KIDEST BAHTA	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/1/08, 6/24/08, 10/07/08, 10/22/08, 11/05/08, 12/04/08, 2/10/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11 and 13-28 are rejected under 35 U.S.C. 102(e) as being anticiapted by Van Hook et al. (US 6,342,892).

Regarding claims 1-11 and 13-28, Van hook discloses,

1. A dedicated, hardware-based Physics Processing Unit (PPU), comprising: a vector processor adapted to perform multiple, parallel floating point operations to generate physics data (column 18, lines 8-11); and a data communication circuit adapted to communicate the physics data to a host (column 16, lines 7-9).

2. The PPU of claim 1, wherein the host comprises a Central Processing Unit (CPU), and the PPU further comprises: a PPU Control Engine (PCE) receiving commands from the CPU and controlling communication the physics data from the PPU to the host (Fig. 5, Fig. 2).

3. The PPU of claim 2, wherein the PPU further comprises: an external memory and an internal memory; and a Data Movement Engine (DME) controlling the movement of data between the external memory and the internal memory in response to instructions received from the PCE (Fig. 5, column 15, lines 1-3).

4. The PPU of claim 3, further comprising: a Floating Point Engine (FPE) performing multiple, parallel floating point operations on data stored in the internal memory (column 18, lines 8-11).

5. The PPU of claim 4, wherein the internal memory is operatively connected to the DME, and further comprising: a high-speed memory bus operatively connecting an external high-speed memory to at least one of the DME and the FPE (column 22, lines 13-15; column 17, lines 17-19; column 18, lines 8-11).

6. The PPU of claim 5, wherein the internal memory comprises multiple banks allowing multiple data threading operations (column 19, lines 41-50).

7. The PPU of claim 3, wherein the PCE comprises control and communication software stored in a RISC core (column 19, lines 60-67).

8. The PPU of claim 5, wherein the internal memory comprises first and second banks,

and wherein the DME further comprises: a first unidirectional crossbar connected to the first bank (column 2, lines 15-39); a second unidirectional crossbar connected to the second bank (column 2, lines 15-39); and, a bi-directional crossbar connecting first and second crossbars to the external high-speed memory (column 4, lines 14-22).

9. A dedicated, hardware-based Physics Processing Unit (PPU) connected within a system to a Central Processing Unit (CPU) and comprising: an external memory storing data; and, an Application Specific Integrated Circuit (ASIC) implementing a vector processor adapted to perform multiple, floating point operations (column 18, lines 8-11; column 16, lines 7-9; column 13, lines 13-16; column 8, lines 39-46).

10. The PPU of claim 9, wherein the system comprises a Personal Computer (PC); and wherein the PPU comprises an expansion board adapted for incorporation within the PC, the expansion board mounting the ASIC and the external memory (column 13, lines 13-16).

11. The PPU of claim 10, further comprising circuitry enabling at least one data communications protocol between the PPU and CPU (Fig. 2).

13. The PPU of claim 11, wherein the ASIC comprises a PPU Control Engine (PCE) receiving commands from the CPU and controlling data communications between the PPU and PC (Fig. 5).

14. The PPU of claim 13, wherein the ASIC further comprises: an internal memory (Fig. 2); and a Data Movement Engine (DME) controlling the movement of data between the external memory and the internal memory in response to instructions received from the PCE (column 19, lines 61-67; column 20, lines 1-8; column 61).

15. The PPU of claim 14, further comprising: a Floating Point Engine (FPE) performing multiple, parallel floating point operations on data stored in the internal memory (column 18, lines 8-11 and column16, lines 7-9).

16. The PPU of claim 15, wherein the internal memory is operatively connected to the DME, and further comprising: a high-speed memory bus operatively connecting the external memory to at least one of the DME and the FPE (Fig. 5, column 18, lines 8-11).

17. The PPU of claim 16, wherein the internal memory comprises multiple banks allowing multiple data threading operations (Fig. 5).

18. The PPU of claim 17, wherein the internal memory further comprises: an Inter-Engine memory transferring data between the DME and FPE (column 19, lines 60-67).

19. The PPU of claim 18, wherein the internal memory further comprises: a Scratch Pad memory (Fig. 6; column 19, lines 41-50).

20. The PPU of claim 14, further comprising a command packet queue transferring command packets from the PCE to the DME (column 19, lines 61-67; column 20, lines 1-8).

21. The PPU of claim 15, wherein the FPE comprises a plurality of Vector Floating-point Units (column 18, lines 8-11).

22. The PPU of claim 21, wherein at least one of the command packets defines a vector length of variable length (column 8, lines 39-46).

23. The PPU of claim 15, wherein the DME comprises a plurality of Memory Control Units (MCUs) and a Switch Fabric connecting the MCUs to the external memory (Fig. 5); and, wherein the FPE comprises a plurality of Vector Processing Engines (VPEs) receiving date from at least one of the MCUs via a VPE bus (.

24. The PPU of claim 23, wherein each Vector Processing Engine (VPE) comprises a plurality of Vector Processing Units (VPUs) receiving data from the VPE bus (column 17, lines 30-42).

25. The PPU of claim 24, wherein each VPU comprises: a dual bank Inter-Engine Memory (IEM) receiving data from the VPE bus (column 19, lines 61-67); one or more

data registers receiving date from the IEM under the control of an associated Load/Store Unit; and an Execution Unit performing parallel floating point operations (column 2, lines 15-39, column 4, lines 14-22).

26. The PPU of claim 23, wherein at least one command packet received from the PCE defines a vector length of variable length (column 8, lines 39-46).

27. The PPU of claim 23, wherein the Switch Fabric comprises at least one crossbar circuit (column 2, lines 15-39, column 4, lines 14-22).

28. The PPU of claim 24, wherein each VPU is dynamically re-configurable (element 420).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook, as applied to claims 9-11 above, in view of Intel (Intel PCI and PCI Express; note that the subject matter relied upon in the reference is dated).

Claim 12, Van Hook does not disclose that the CPU and PPU communicate via at least one selected from a group of physical interfaces consisting of: USB, USB2, Firewire, PCI, PCI-X, PCI-Express, and Ethernet. On the other hand, Intel discloses of a PCI interface, or alternatively, of a PCI- Express interface (pages 2-3, PCI, PCI Express). The PCI interface is a tenfold performance gain over ISA, has plug-and-play capabilities, and is processor agnostic and flexible (Intel, page 2). Alternatively, the PCI-Express interface supports important features such as power management and the ability to handl both host-directed and peer-to-peer data transfers (Intel, page 3).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a PCI interface, or alternatively, a PCI-Express interface, for the above reasons. Alternatively, one rationale that may be used to support the conclusion of obviousness is simple substitution of one known element for another to obtain predictable results, and it is noted in Figure 2 of Van Hook as modified that there exists a bus that connects the CPU and the PPU.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed Kidest Bahta whose telephone number is 571-272-3737.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Paul Rodriguez can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application information Retrieval IPAIRI system. Status information for published applications may be obtained from either Private PMR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-fee).

/Kidest Bahta/

Primary Examiner, Art Unit 2123